



roedal arabear

Figure 4A

	stage D	stage C	stage B	stage A
15				
14				SUB [3]
10 11 12 13 14 15				SUB [2]
12				SUB [1]
11				SUB [0]
10				ADD ADD [1]
6				ADD [1]
80				ADD [0]
7				
9				
S				
4				
က		_		
2				
-				
0				

current pointer = 8
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 11 carry = false fwrap = false stage swap mux selects stage A

shift = 0

Instruction Buffer Stage Selection Example: Case 1

roenzazz. Ozeneo

Figure 4B

	stage D	stage C	stage B	stage A
15				ADD [2]
14				ADD ADD ADD [0]
10 11 12 13 14 15				ADD [0]
12				
1				
10				
6				
80				
7				
9		_		
2				
4				
က			SUB [3]	
7			SUB [2]	
~			SUB [1]	
0			SUB [0]	

current pointer = 13
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 0 carry = true fwrap = false stage swap mux selects stage B

shift = 1

Instruction Buffer Stage Selection Example: Case 2

Figure 4C

TOEDSEE SEESPO

	stage D	stage C	stage B	stage A
15				ADD [1]
10 11 12 13 14 15				ADD ADD [0]
13		·		
12				:
=				
10				
6				
æ				
~				
9				
5				
4			SUB [3]	
က			SUB [2]	
2			SUB [1]	
-			SUB [0]	
0			ADD (2)	

current pointer = 14
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 1 carry = true fwrap = true stage swap mux selects stage B

shift = 1

Instruction Buffer Stage Selection Example: Case 3

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Figure 4D

	stage D	stage C	stage B	stage A
15				
10 11 12 13 14 15			SUB [3]	
13			SUB SUB SUB SUB [0] [1] [2] [3]	
12			SUB [1]	
1			SUB [0]	
10				
6				
æ				JCC JCC [0] [1]
7				၁၁ ြ
9				
2		- 		
4				
က				
2				
-				
0				

current pointer = 7
instruction length = 2
BTAC branch indicator[7] = true
target address[0:3] = 11

next pointer = 9 carry = false fwrap = false stage swap mux selects stage B

shift = 1

Instruction Buffer Stage Selection Example: Case 4

Figure 4E

LOEDSBEE LOZOWOL

	stage D	stage C	stage B	stage A
15				JCC [1]
14	:		SUB [3]	JCC JCC [0] [1]
12 13 14			SUB SUB [1] [2]	
12			SUB [1]	
10 11			SUB [0]	
10				
6				
80				
7				
9				
2				
4				
က				
2				
-				
0				

current pointer = 14 instruction length = 2 BTAC branch indicator[14] = true target address[0:3] = 11

next pointer = 0 carry = true fwrap = false stage swap mux selects stage B

shift = 1

Instruction Buffer Stage Selection Example: Case 5

Figure 4F

TOEDSG. TESSESOL

SUB [2] SUB [1] 12 SUB [0] 7 10 တ œ 9 2 4

က

8

0

35C E

stage D

15

4

13

stage C stage B

SUB [3]

stage A

၁၁၄ [0]

current pointer = 15	instruction length = 2	BTAC branch indicator[15] = true	target address[0:3] = 11
current pointer = 15	instruction length = 2	BTAC branch indicator[15]	target address[0:3] = 11

next pointer = 1 carry = true fwrap = true

stage swap mux selects stage C

shift = 2

Instruction Buffer Stage Selection Example: Case 6